

REMARKS/ARGUMENTS

This is in response to an Office action dated 01/24/2007 having a statutory period of response set to expire on April 24, 2007.

Status

Claims 23-32 and 37-42 are pending

Claims 37-42 are allowed

Claims 23-30 and 32 are rejected

Claim 31 is objected to

Claim Rejections under 35 USC § 102

Claims 23-30 and 32, are rejected under 35 U.S.C. 102(b) as being anticipated by Katzenstein (US Patent 5,245,332).

As stated in the Office Action, “Regarding claims 25 and 27, Katzenstein discloses an RE transponder comprising an antenna system characterized by:

a programmable load (see abstract) connected to the antenna system for transmission modulation (see col.12 lines 1-2); and.

a programmable load (see abstract) connected to the antenna system for transmission modulation (see col. 12 lines 1-2); and

a power supply and level shifters connected to the programmable load, wherein voltage changes in the power supply dynamically vary a magnitude of the programmable load according to power available in the transponder (see col. 13 lines 20-61).

Regarding claim 23 and 28, Katzenstein discloses a plurality of first output stage transistors (see 72, 76, 78 fig.4) connected to a first terminal (see 81, fig.4) of the antenna system;

a corresponding plurality of second output stage transistors (see 72, 76, 78, fig.4) connected to a second terminal (see 83, fig.4) of the antenna system; and

control logic for determining which ones of the first output stage transistors and which ones of the second output stage transistors are used to modulate the antenna system (see col.8

Regarding claims 24 and 29, Katzenstein discloses an EEPROM storing programmed settings for driving the control logic (see col.13 lines 15-16).

Regarding claims 26 and 32, Katzenstein discloses a gate for disconnecting modulation of the antenna system in response to a reset signal (see col.10 lines 64).

Regarding claim 30, Katzenstein discloses control logic connected for modulating the dynamically variable load, wherein the control logic has a control signal input formed in a gate by logically combining a system clock signal and a data stream (see col. 8 lines 32-45).

Independent Claim 25 has been amended to include claim 23 and the limitation of a sync delay circuit for delaying the system clock signal in order to synchronize the system click signal with the data stream.” Since the latter limitation is not taught or suggested by Katzenstein, claim 25 should be allowable.

Claims 24 and 26 depend upon claim 25 and should also be deemed allowable.

Claims 31 was objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 31 has been amended to include claims rejected base claim 27 and intervening dependent 30. Accordingly, claim 31 should be deemed allowable.

Claims 28, 29 and 32 depend upon claim 31 and should therefore also be deemed allowable.

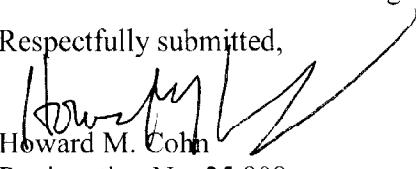
Claims 37-42 were allowed.

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Amdt. Dated 04/19/2007
Reply to Office action of January 24, 2007

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.
If any matter still needs to be resolved, the Examiner is invited to contact the undersigned.

Respectfully submitted,


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